# AN 80/160 GHZ BROADBAND, FIXED-TUNED, BALANCED FREQUENCY DOUBLER

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## ABSTRACT

We report on the development of a high-power, broadband, fixed-tuned 80/160 GHz frequency doubler. The design is based on a similar 40/80 GHz doubler which exhibited a measured 3 dB bandwidth of 17 % and peak efficiency of 48% at an output power of 100 mW[1]. Simulations for the new 80/160 GHz doubler indicate similar bandwidth and efficiency. The focus of this paper is the design and simulation of the 80/160 GHz doubler. Test results will be presented at the conference.

## INTRODUCTION

Many millimeter-wave and submillimeter-wave LO sources in use today comprise a low noise fundamental microwave source followed by a chain of frequency multipliers and amplifiers. Current state-of-the-art frequency multipliers tend to exhibit relatively high Q's and typically employ mechanical tuners to provide increased bandwidth. It is desirable to eliminate these tuners and yet maintain broadband operation.

The 80/160 GHz doubler is essentially a scaled version of the 40/80 GHz doubler, which was derived from an 87/174 GHz doubler reported by Erickson [2]-[4]. Figs. 1,2 show sketches of the 40/80 GHz and 80/160 GHz doublers.

There are no adjustable mechanical tuners in these designs. The center conductor for a TEM line, an output waveguide probe and an RF blocking filter for the DC bias line are photolithographically formed on a quartz substrate. This allows for a high degree of control

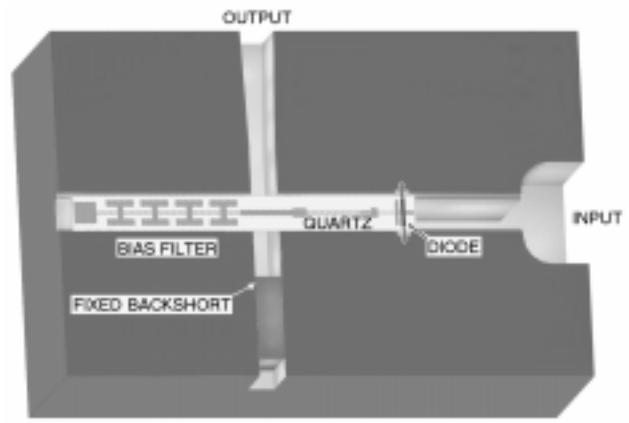


Fig. 1. 40/80 GHz planar balanced doubler.

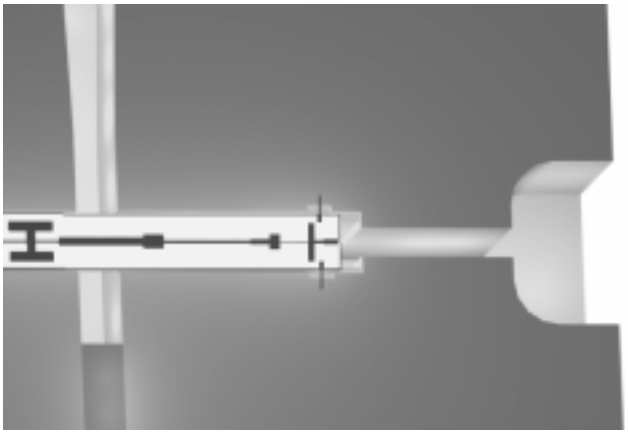

Fig. 2. Enlarged view of the 80/160 GHz planar balanced doubler showing the modified reduced height input waveguide. The varactor is not shown in order to reveal the mounting pads and bond wires.

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of the center conductor dimensions and therefore substantial control over the second harmonic embedding impedance. The quartz circuit sits in a split waveguide block. The 80/160 GHz block is essentially a scaled version of the 40/80 GHz design with two notable exceptions; i) the overall length of the varactor chip could not be scaled down by a factor of two and thus the reduced height waveguide at the varactors is not a true scaled version of the 40/80 GHz block and, ii) there is a further reduction in the waveguide height between the varactors and the full height input guide in the 80/160 GHz version which does not appear in the 40/80 GHz version.

The 40/80 GHz doubler employed a linear array of 6 GaAs planar Schottky varactors with an epitaxial layer doping of $1x10^{17}$ $cm^{-3}$ and anode diameters ranging from 12-14 µm. The 80/160 GHz doubler employs a linear array of 4 GaAs planar Schottky varactors with an epitaxial layer doping of $2x10^{17}cm^{-3}$ and anode diameters ranging from 4-7 µm. The series resistance can be calculated using the method described in [5] to be 0.8 Ω and 1.6 Ω per varactor for the 13 µm and 6 µm anodes respectively. However, measured values of series resistance are typically found to be somewhat higher than calculated values. The calculations described in [5] assume a high degree of rotational symmetry in the area around the anode and ohmic contact. This symmetry is generally applicable for whisker contacted devices, but may lead to artificially low values of series resistance in planar devices. There are also a number of other ohmic loss mechanisms in the planar package including skin effect losses in the finger and losses in the bulk semi-insulating GaAs substrate.

Since these multipliers do not employ any mechanical tuners, it is imperative that the frequency dependent embedding impedances of the circuit be well understood. Hewlett-Packard's High Frequency Structure Simulator (HFSS) was used to model the quartz circuit, varactor package and waveguide block. HFSS ports were attached to probes at each anode to determine the individual varactor embedding impedances. A large number of geometrical perturbations of the waveguide, varactor and quartz circuit were simulated in HFSS and analyzed to determine a range of embedding impedances that could be provided by the circuit. We compared the circuit impedance data to the optimum varactor embedding impedance data and chose a circuit and block design which provided the best match over the widest bandwidth.

## MEASURED/SIMULATED RESULTS

We present a brief review of the measured results for the 40/80 GHz doubler and a comparison of the simulated and measured performance [1]. We also present simulated results for the 80/160 GHz doubler. Using some caution, a rough estimate of the expected performance of the 80/160 GHz doubler can be extrapolated from this data.

The graph in Fig. 3 shows measured output power and efficiency versus input power for the 40/80 GHz doubler using varactor chips with 12 µm and 13 µm anodes. The measured peak efficiency was 48 % at an output frequency of 82 GHz. The zero biased junction capacitance was calculated to be approximately 120 fF for the 12 µm anodes and 140 fF for the 13 µm anodes.

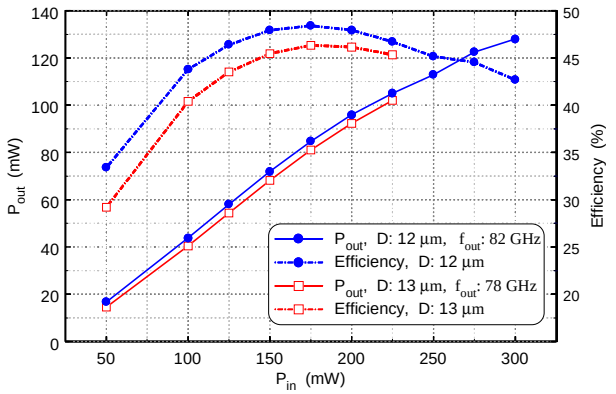


Fig. 3. Measured output power and efficiency versus input power for two different varactor chips (40/80 GHz doubler).

Fig. 4 shows measured output power versus output frequency for the 12 µm and 13 µm anode varactors. The input power for this measurement was 200 mW. The measured 3 dB fixed-tuned bandwidth was approximately 17 %.

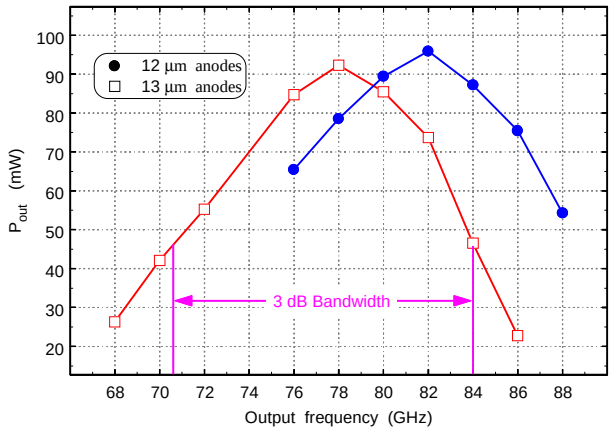


Fig. 4. Measured output power versus output frequency for $P_{in}$ = 200 mW (40/80 GHz doubler).

Harmonic balance simulations were compared to the measured results. The simulations used 5 harmonics, with the embedding impedances at the first (fundamental) and second harmonics obtained from HFSS simulations of the circuit while shorts were used at the higher harmonics. For the 40/80 GHz doubler, the measured and simulated fixed-tuned bandwidths were both 17 %, but the measured output power was 1.8 dB down from the simulated result. The discrepancy in the measured and simulated output power is eliminated if a series resistance of 2.5 Ω is used instead of the calculated 0.8 Ω.

The graph in Fig. 5 shows simulated output power and efficiency versus input power for the 80/160 GHz doubler at an output frequency of 160 GHz. The harmonic balance simulations used HFSS simulated embedding impedances and a GaAs chip containing four varactors with nominal 7 µm diameter anodes ($C_{j0}$ = 63 fF) and a reverse breakdown voltage of 10 V. We also used an assumed value of 3 Ω/varactor in the simulations rather than the calculated 1.6 Ω. The peak

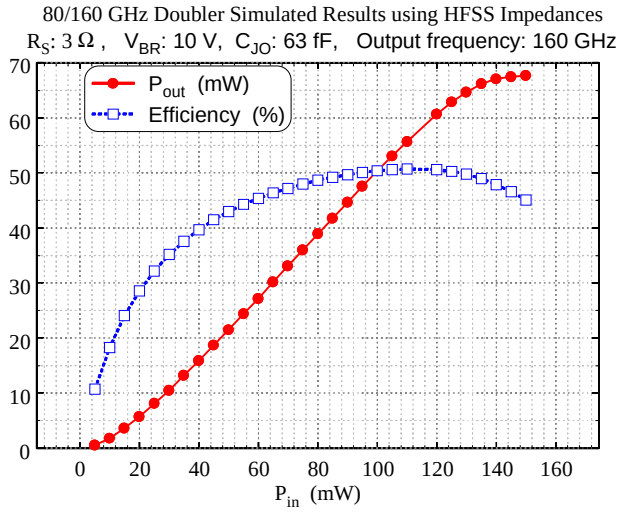


Fig. 5. Simulated output power and efficiency versus input power at 160 GHz.

simulated efficiency was 51 % at $P_{in}$=110 mW.

The graph in Fig. 6 shows simulated output power and efficiency versus output frequency for an input power of 80 mW. The simulation environment was the same as described in the preceding paragraph. The peak output power was 40 mW at 160 GHz. The corresponding efficiency is approximately 50 %.

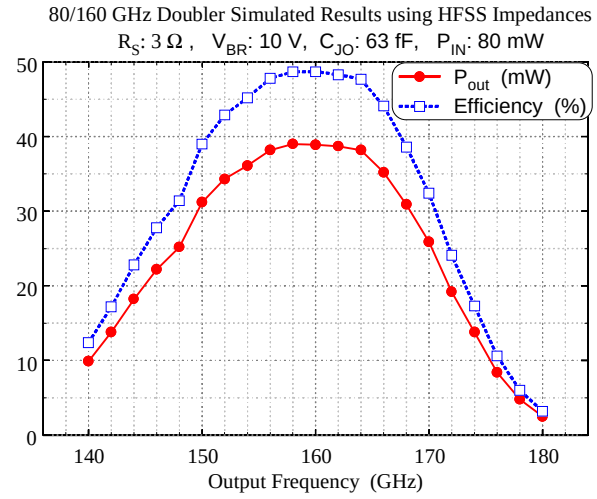


Fig. 6. Simulated output power and efficiency versus frequency for an input power of 80 mW.

## CONCLUSION

We have developed a broadband, fixed-tuned, high power 80/160 GHz frequency multiplier. The doubler is mechanically rugged, easy to assemble and relatively inexpensive. The design is based on a 40/80 GHz prototype which exhibits record fixed-tuned bandwidth and output power [1]. For the 40/80 GHz doubler, the measured and simulated fixed-tuned bandwidths were both 17 %, but the measured output power was 1.8 dB down from the simulated result. The discrepancy in the measured and simulated output power is eliminated if a series resistance of 2.5 Ω is used instead of the calculated 0.8 Ω.

Simulations for the 80/160 GHz doubler show efficiency and bandwidth similar to the 40/80 GHz design for the case of an assumed 3 Ω per varactor series resistance. Circuit losses in the waveguide, microstrip and quartz were not included, but these losses are expected to be less than 1 dB. The circuit losses should have little effect on the bandwidth but will slightly reduce the efficiency and output power.

## ACKNOWLEDGMENTS

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